12bit UnderSampling ADC TEST Solution

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ADC 개요

- Resolution : 12bit
- Differential Linearity error: ± 1.0LSB
- Integral Linearity error: ± 4.0LSB
- Maximum conversion rate: 25MHz
- Wide input bandwidth up to 50MHz
- Power supply: 3.3V
- Offset binary or two’s complement data format
Basic for ADC TEST

- **Static test**
  - DLE (Differential Linearity Error)
  - ILE (Integral Linearity Error)
  - Offset Error

- **Dynamic test**
  - THD (Total Harmonic Distortion)
  - SNR (Signal to Noise Ratio)
  - SFDR
Static TEST

\* DLE, ILE, Offset Error

![Graph showing DNL and INL error](image)
Dynamic TEST

- SNDR, THD, SFDR

SNR (dB) = 20 x log $\frac{E_F}{E_N}$

THD (dB) = 20 x log

$\sqrt{\frac{E_{H2}^2 + \ldots + E_{H9}^2}{E_F}}$

THD+N (dB) = 20 x log

$\sqrt{\frac{E_{H2}^2 + \ldots + E_{H9}^2 + E_N^2}{E_F}}$

SINAD = SNR + D = $\frac{\text{Signal} + \text{THD} + N}{\text{THD} + N}$
UnderSampling

- Sampling Freq. < Input Freq.
- Requirements for undersampling
  - Broad bandwidth for Input
  - Coherent sampled output for input
What is the most important for high resolution ADC TEST

- Pure single tone analog input
- Low jitter input clock
- Low noise power source
- Coherence sampling
- Qualified PCB
Qualified PCB

- Locate all bypass capacitors as close to the device as possible
- Multilayer boards with separate ground and power planes produce the highest level of signal integrity
- Route high-speed digital signal traces away from sensitive analog traces
- Route clock away from actual analog inputs and other digital signal lines
How can we make pure input source?

- Band pass filter for ADC input
Coherent Testing

\[ F_s \times M_c = F_0 \times N \]

http://www.maxim-ic.com/appnotes.cfm/appnote_number/729
What is the problem?

- SNDR = 54dB, THD = 64dB at ATE
- SNDR = 63dB, THD = 78dB at Bench
Spectrum Leakage

\[ F_s \cdot M_c = F_o \cdot N \]

Spectrum leakage
Effect of hanning

- Good frequency resolution and reduced spectrum leakage

Rectangular window  hanning window
Effect of Windowing

Rectangular Window

hanning Window
Clock Jitter Vs SNR

* Catalyst Instruction Manual Version8.3, Teradyne co
Effect of Clock

High jitter clock

low jitter clock
Effect of Filter

No Bandpass filter

Bandpass filter
Optimization for ATE

- 50MHz bandpass filter
- Hanning window
- Low jitter clock (3ps)

SNDR: 64.02dB
THD: 75.46dB
Conclusion

- Qualified PCB
- Pure Single tone input
- Coherence
- Low jitter clock